A Ka-BAND GaAs POWER MMIC

M. Kobiki, Y. Mitsui, Y. Sasaki, M. Komaru, +K. Seino and +T. Takagi

LSI Research and Development Laboratory,
+Information Development Laboratory, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo 664, Japan

ABSTRACT

A Ka-band GaAs power MMIC with source island via-hole PHS structure and monolithic power divider /combiner circuits was developed and reliability study was performed. This source island via-hole technique successfully reduced both thermal resistance and source parasitic inductance of the MMIC. The 3200 μm MMIC gave power output at 1dB gain compression of 1.1 W, linear power gain of 4.0 dB and power added efficiency of 10.8 % at 28 GHz.

No failure was observed in the temperature cycling, the DC running and the high temperature storage tests.

INTRODUCTION

Recent advances in GaAs power FET development have brought device operation to K-band frequencies.[1, 2, 3] On the other hand, demands for GaAs power FET's operable at Ka-band are increasing for satellite communication system applications.

However, at Ka-band, dimension of a high-power FET chip becomes comparable to the signal wavelength and it becomes much more difficult to feed a microwave signal uniformly to each unit cell of such a large FET. Moreover, without reducing thermal resistance and parasitic reactances such as series source inductance of the chip it is difficult to achieve practical operation of the power FET's.

Discrete FET processing technique using usual via-hole grounding is therefore inapplicable to such high frequency power GaAs FET's with extremely low input impedance.

This paper describes a newly developed 28 GHz-band 1 W GaAs power MMIC for satellite communication systems. In this study, following two approaches were adopted to overcome gain and power reductions of FET's at Ka-band frequencies. Namely,

(1) Each island source electrode of the FET's was grounded directly through Au plated thin via-holes, which realizes extremely low source inductance and excellent heat transfer characteristics.
(2) Monolithic planar divider/combiner technique was developed to achieve impedance, phase and amplitude matching for each unit cell.[4]

DEVICE STRUCTURE AND WAFER PROCESSING

Figure 1 shows view of a completed 3200 μm gate high power MMIC chip. Chip size is 2.1X1.4 mm^2. Four unit FET cells are connected with monolithic divider/combiner circuits. The gate width of the unit FET cell, which consists of eight 100 μm gate fingers, was determined in considering internal phase and amplitude unbalances. A thickness of a GaAs substrate was chosen to be 30 μm on the basis of a tradeoff of factors such as parasitic source inductance, conductor loss circuitry and thermal considerations. Monolithic divider/combiner circuits, which consist of low impedance transmission lines and epitaxial isolation resistors, were optimally designed to realize well-balanced operation of the each cell. Figure 2(a) shows an enlarged microphotograph of the FET portion. Figure 2(b) is a cross-section in A-A' plane of Fig.2(a).

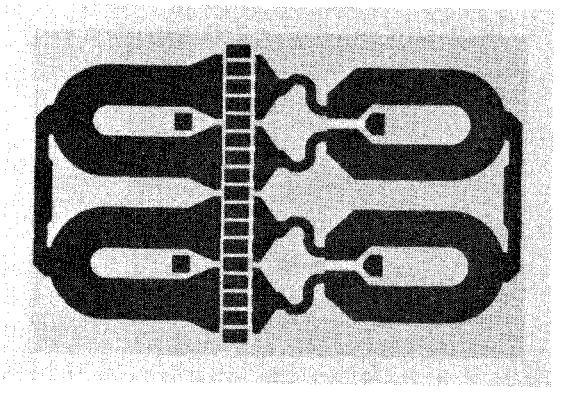

Fig.1 Microphotgraph of a 4 cell MMIC chip

The fabrication steps for this MMIC are as follows;

(a) The fabrication procedures for the FET portion are similar to those for conventional micro-

wave MESFET's using epitaxial wafer.

(b) Small holes with a depth of 30 μm are formed at each island source electrode from the front surface by chemical etching. The holes are electroplated by Au film with 5 μm thick.

(c) The whole area of the back surface is etched until the bottom of the Au plated holes formed from the front surface is appeared.

(d) In order to reduce the thermal resistance and to ease the chip handling, the selective Au plated heat sink (PHS) of 70 μm thick is formed on the back surface.

(e) Finally, each chip is separated from the wafer by selective etching.

Using this technique, the thickness variation of the substrate could be accurately controlled within 5 μm over the 2" wafer. Consequently, the characteristic impedance variation of the transmission line from the designed value was minimized to less than 10 %.

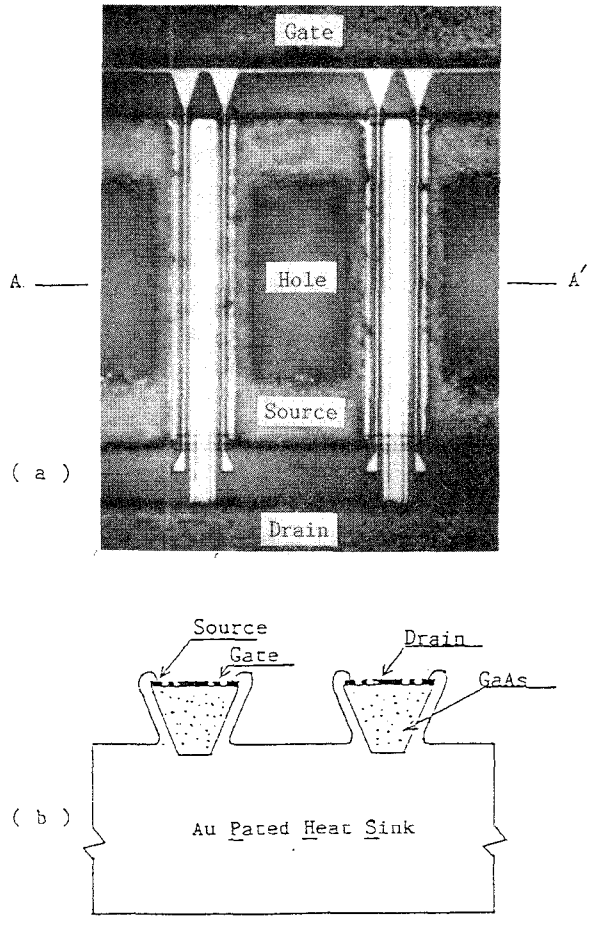

Fig.2 (a) Microphotgraph of the FET portion and (b) a cross section in A-A' plain

PERFORMANCE

Saturation current, pinch-off voltage and transconductance were typically 1.15 A, -4.0 V and 170 mS/mm, respectively. The breakdown voltage at a reverse current of 100 μA was higher than 16 V.

Figure 3 shows distribution of the thermal resistance of the packaged MMIC's compared with that of conventional air bridged FET's. Typical thermal resistance of the air bridged 1600 μm FET with 200 μm thick substrate was 32 °C/W, whereas that of 1600 μm MMIC's was improved to 12 °C/W. Typical thermal resistance of the 3200 μm MMIC chip was 4 °C/W.

An equivalent circuit was derived by curve fitting to the measured small signal S-parameters. Figure 4 shows an equivalent circuit for typical 800 μm monitor FET. The drain-to-source voltage and the gate-to-source voltage were 8.0 V and -1.5 V, respectively. The estimated source inductance was in the range of 0.6 to 2.5 pF which was one-order magnitude smaller than that reported in Ref.2.

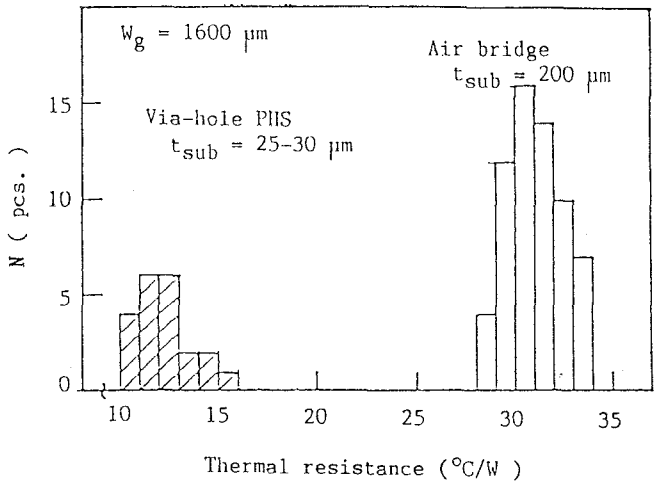

Fig.3 Distribution of the thermal resistance

Figure 5 shows typical input-output characteristics of the power MMIC compared with that of 800 μm monitor FET at 28 GHz. The 3200 μm MMIC gave power output at 1dB compression of 1.1 W, linear power gain of 4.0 dB and power added efficiency of 10.8 %. While for the 800 μm monitor FET, 0.3 W, 5.0 dB and 16.9 % were achieved.

Figure 6 shows a power output per unit gate width, linear power gain and power added efficiency at 28 GHz versus the total gate width. It is noted that the power output per unit gate width is as as high as 0.35-0.37 W/mm, indicating that the excellent power combining efficiency as high as 80 % can be succsessfully realised by using this MMIC technique.

Figure 7 shows a typical frequency responce of output power of 3200 μm MMIC. A power output higher than 1.0 W with 3 dB gain was obtained over the frequency range of 27-28.5 GHz.

Figure 8 shows a result of temperature cycling test for packaged MMIC's. Monitored DC parameters were saturation current, transconductance, pinch-off voltage and breakdown voltage. all the deviation ratioes to the starting values of DC parameters were within less than 10 %. And no failure was observed.

Moreover, failure was not observed even after 1000 hrs in a DC running test at the channel temperature of 150 ℃ and a high temperature storage (200 ℃)test. The results indicate that this source island via-hole PHS MMIC's were proved to be feasible as a highly reliable devices.

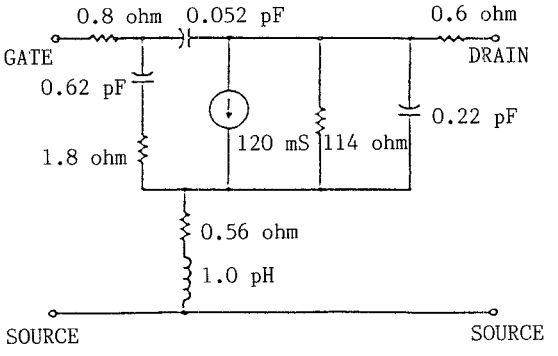

Fig.4 Typical equivalent circuit of the unit FET cell (800 μm)

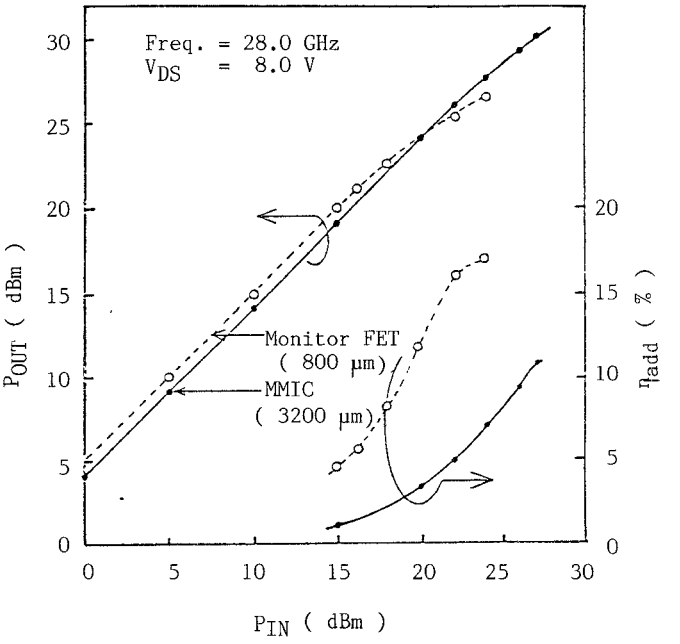

Fig.5 Typical input-output characteristics of the MMIC and the monitor FET

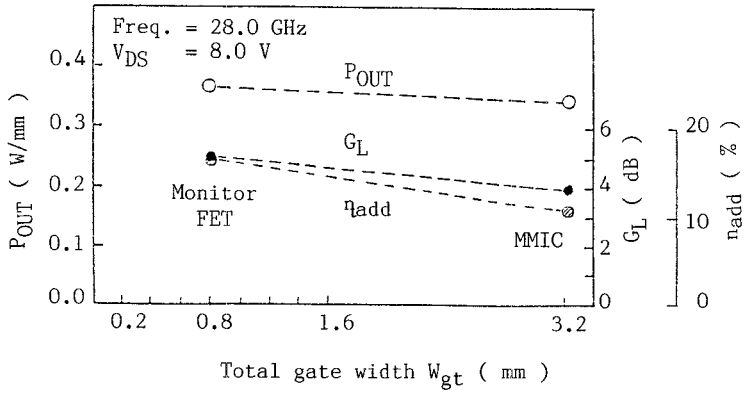

Fig.6 P_{1dB} per unit gate width, G_L and η_{add} versus the total gate width

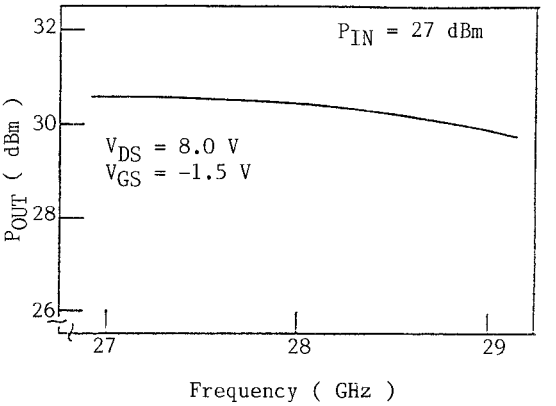

Fig.7 Frequency responce of the MMIC

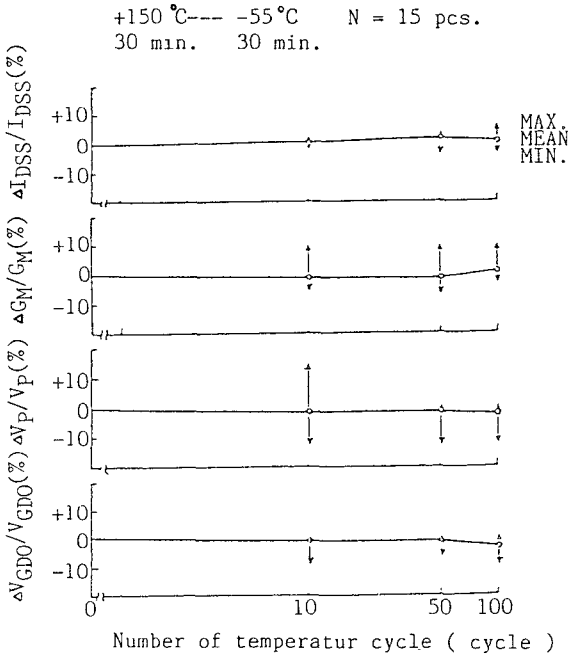

Fig.8 Result of temperature cycling test

CONCLUSION

A Ka-band GaAs power MMIC with via-hole PHS structure and monolithic power divider/combiner circuits was developed for application of satellite communication systems. Power output of 1.0 W with 3 dB gain was realized over a frequency range of 27-28.5 GHz. These MMIC's were proved to be feasible as a highly reliable device. These results indicate that the MMIC possesses the performance adequate for practical use in the systems.

ACKNOWLEGEMENT

The authors would like to thank Mr.K.Fujikawa and Dr.F.Takeda for their helpful discussions and encouragements throughout this work.

They also thank Mr.A.Saeki, Drs.M.Nakatani and O.Ishihara for their valuable discussions.

A part of this work was supported by Ministry of International Trade and Industry of Japan.

REFERENCES

1 J.Goel, "A K-band GaAs FET amplifier with 8.2 W output power" IEEE Trans. MTT, vol. MTT-32, NO.3 pp.317-324, March, 1984.

2 Y.Hirachi, et.al., "A packaged 20 GHz 1-W GaAs MESFET with a novel via-hole plated heat sink" IEEE, Trans. MTT, vol. MTT-32, NO.3, pp.309-316 March, 1984.

3 J.Sone, et.al., "K-band high power GaAs FET amplifiers" IEEE Trans. MTT, vol. MTT-29, NO.4, pp.309-313, April, 1981.

4 K.Seino,et.al., "A 1 watt 28 GHz band amplifier using clustered FET's" this symposium.